Integration Concepts for Multi-Standard Wireless Transceivers

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Abstract. Modern solutions of wireless communication systems require multi-standard and multi-band functionality for future software defined radio and agile radio products. The high number of wireless standards implemented in mobile devices (like GSM/EDGE, UMTS, LTE, 5G, Wi-Fi, GPS, Wireless HD, Wireless USB, NFC or Bluetooth) creates a number of challenges, which are not covered by "classical" radio-frequency (RF) circuit concepts and analog-mixed signal design methodologies only. Problems like strong interference between the different RF frontends, a complex interface between the RF integrated circuit and external components like filters or antennas, as well as limitations of available power, chip area, PCB area and mainly costs needs to be solved for future products. This leads to the necessity of new RF frontend concepts leveraging reconfigurable RF building blocks using "digitally assisted RF" and sampling receiver concepts with interference cancelation strategies together with heterogeneous integration methods. The research activities of the Josef Ressel Center (JRC) for Integrated CMOS RF Systems and Circuits Design (Interact) at Carinthia University of Applied Sciences (http://www.jrz-interact.at/) are directly aligned to these aspects and are summarized in this document.

Keywords: RF transceivers, multi-standard, subsampling, RFIC, tunable LNA

1 Introduction

The development of modern wireless communication devices is dominated by stringent multi-standard and multi-band requirements. The high number of wireless voice and data communication standards implemented in mobile devices is challenging not only for IC design, but also for package and board development. The main challenge of future mobile devices will be, on the one hand, the reduction of integrated devices and PCB area by using optimized System-on-Chip (SoC) and System-in-Package (SiP) technologies to achieve lower costs. On the other hand the coexistence of a high number of RF frontends in a multi-band transceiver IC causes problems, which needs to be solved in future. The trend goes to single on-chip radio architec-

tures. This leads to the requirement of frequency agile, multi-mode, multi-standard RF architectures, based on Systems-on-Chip solutions for nanoscale CMOS.

Focus 1: *New RF frontend concepts are researched in the Josef Ressel Center for Integrated CMOS RF Systems and Circuits Design (JRC - Interact), leveraging reconfigurable building blocks using digitally assisted RF concepts to cope with non-idealities in the RF performance such as gain control, offset control or noise and crosstalk compensation.*

Another strong research trend is shifting the discrete time sampling and quantization of the input signal as far as possible to the input of the RF receiver chain called as software-defined-radio. This offers the highest flexibility, as it can select and process any signal band or channel in the digital domain [1]. On the other hand a Nyquist rate sampling and quantization in the RF domain demands for very stringent performance requirements resulting in very high power dissipation. Therefore an intermediate solution is researched in the JRC - Interact where signal discretization by a sampler is shifted to the RF domain in front of the mixer, while the quantization with an Analog-to-Digital Converter (ADC) is still in the baseband. This enables innovative mixing concepts like sub-sampling down conversion [2], where the RF signal is sampled at a lower sampling rate. Mixing and filtering can be done at lower frequency by discrete time charge domain switched capacitor circuits, which promise flexible and power efficient RF frontend solutions.

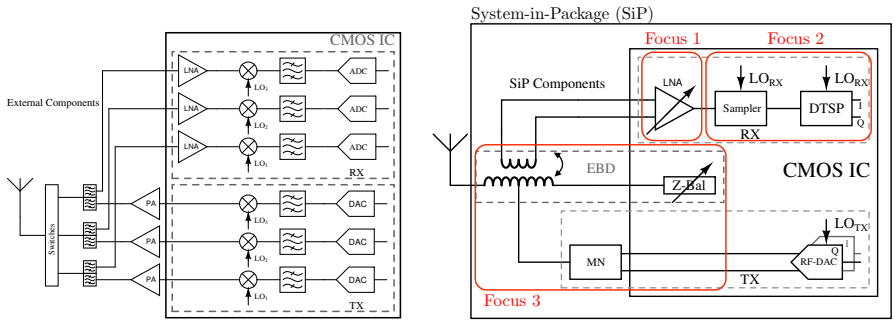
Focus 2: *The concept development, design and implementation of sub-sampling based receiver frontends is a main focus of research in the JRC - Interact.*

To realize the integration for future mobile voice and data communication devices, a combination of monolithic and heterogeneous integration strategies need to be considered. The monolithic integration follows the classical More - More approach [3] leveraging the scaling advantages of newest nano-technologies, by adding RF process add-ons like RF transistors and passive components such as coils, varactors or antennas to the latest available CMOS technology realizing a System-on-Chip (SoC). As an alternative, the heterogeneous integration of external components (eg. power transistors, passive components, switches, duplexers or MEMS filters) can be assembled in a common package avoiding specific printed circuit boards also known as System-in-Package (SiP) or 3D-integration. This leads to strong requirements for new modeling and CAD strategies. A multi-disciplinary co-design will become more and more important for future applications since heterogeneous and monolithic integration of different non-standard components is steadily growing.

Focus 3: *The SiP co-design and optimization of integrated RF transceiver frontends together with passive components like RF filters, baluns and impedance transformation circuits as well the research on new concepts for integrated duplexers are fields of research in the JRC - Interact.*

2 Research Topics

Multi-band and multi-standard operation of modern wireless transceivers, leads to complex, bulky and power hungry implementations. **Fig. 1**a illustrates a state of art wireless transceiver where several Transmitter (TX) and Receiver (RX) chains are required in order to fulfill the specifications. In addition to the large number of parallel components in the CMOS integrated circuit (IC), each chain requires an external high-cost duplexer filter and a Power Amplifier (PA). With the evolution of wireless systems, even more communication standards are being created while maintaining backwards compatibility, therefore the cost, power consumption and complexity of the RF transceivers tend to increase. Also, demand of long battery life time and competitive prices motivates the research on new transceivers concepts.



a. b.

Fig. 1. Traditional wireless transceiver concept for multi-band and multi-standard operation (a.) and Proposed transceiver concept with SiP integrated duplexer RF-DAC transmitter and sub-sampling receiver (b.)

The overall aim of JRC – Interact is research on innovative concepts for receivers, transmitters and System-in-Package (SiP) integration, which provides reconfigurability, wide frequency operation, higher power efficiency and low-cost transceivers. Innovative concepts can be used to create a transceiver architecture presented in **Fig. 1**b with the 3 JRC - Interact research foci indicated with red boxes.

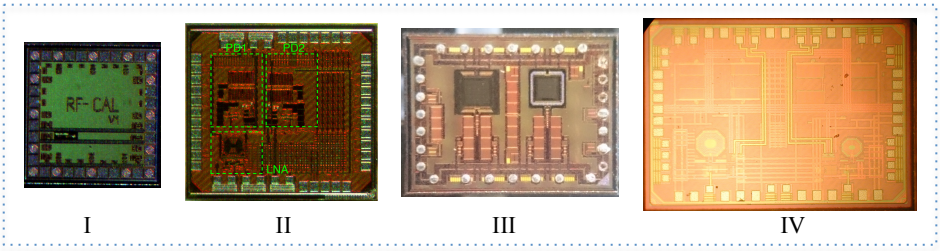
The RX chain is based on a tunable low-noise amplifier LNA (**Focus 1**) and a sub-sampling receiver (**Focus 2**). A tunable-gain and tunable-band LNA relaxes the linearity requirements of wideband LNAs to fulfill the sensitivity performance for various wireless standards. The proposed sub-sampling receiver architecture is based on a RF sample-and-hold circuit (Sampler) followed by Discrete Time Signal Processing (DTSP) for down conversion and filtering. A sub-sampling receiver requires lower power consumption and provides more flexibility for digital signal processing compared to traditional all-analog receivers.

For low-cost applications in the field of IoT, the transmitter TX can be realized as fully integrated high-efficiency digital power amplifier (RF-DAC) to avoid high cost external power amplifiers (PA). An RF-DAC unites in one block the functionality of a Digital-to-Analog Converter (DAC), up-conversion and amplification stage. It has the

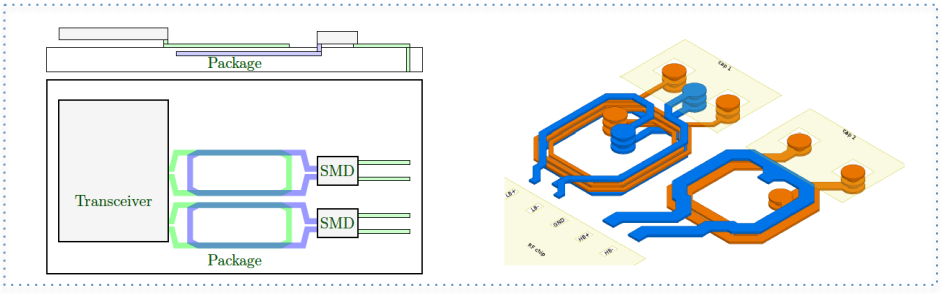
advantage of higher efficiency compared to traditional analog PAs and can be integrated in standard CMOS technology. But still the simplified transceiver concept cannot fully avoid external RF components. For overall system optimization modern SiP technologies can be used providing high-quality, low-cost passive components for matching network MN and electric-balance duplexer EBD (**Focus 3**).

3 Scientific Results

The three focus topics have been intensively researched since April 2014 when the JRC – Interact has been started. Different use-cases and system level specification for the building blocks have been discussed and defined in close cooperation with the industry partner Intel Austria GmbH. A top-down development approach has been followed for the three fields of research starting from system level modeling and design leading to physical circuit level implantation. Consequently each function has been verified by lab measurements on demonstrator IC testchips. For the demonstrator implementation different modern IC technologies have been used like 65nm CMOS, 130nm SOI and 28nm CMOS.



a.)



b.)

Fig. 2. Demonstrator IC's to verify the research on tunable LNAs integrated matching networks and sub-sampling receivers (a.) SiP integration demonstrators for RF matching networks (b.)

A testchip gallery is shown in **Fig. 2**a. The testchip I is a calibration IC which is used to calibrate the lab measurement setup for de-embedding the parasitic effects of evaluation boards or bond-wires. Testchip II is related to research Focus 1 and includes tunable low-noise amplifier circuits (LNAs) together with RF power detector mod-

ules. The measured results have been published in [4], [5], [7], [10] and [11]. The latest research on sub-sampling receiver frontends (research Focus 2) has been verified by the 65nm CMOS demonstrator Testchip IV. First scientific results are published in [6], [13] and [14]. Finally the 130nm SOI Testchip III includes specific passive matching networks and RF switches used for optimized TX frontends. For performance comparison also different integration concepts for RF matching networks has been analyzed. The implementation of an impedance transformation network in SiP technology for a RF-DAC based TX frontend is shown in **Fig. 2**b. For realization a co-design of the CMOS transceiver IC output stage with the in-package transformer is necessary. Different aspects of this heterogeneous RF integration have been published in [8], [9] and [12].

4 Summary

The article gives an introduction to challenges of highly integrated wireless communication frontends, introduces future trends in RF integration and summarizes the research work of the Josef Ressel Center for Integrated CMOS RF Systems and Circuits Design (Interact) at the Carinthia University of Applied Sciences. The work is funded by the Austrian Federal Ministry of Science, Research and Economy and the National Foundation for Research, Technology and Development, which is gratefully acknowledged. New integration concepts of wireless transceiver systems are an essential requirement for future mobile communication and sensor networks like Internet-of-Things (IoT). The presented research topic has therefore a vital impact on future wireless communication, which is a fundamental pillar of our society with a high economic importance for Austrian microelectronics and communication industry.

The focus of a JRC is mainly defined by application-oriented research. Therefore the active cooperation with industry partners is a fundamental requirement. The JRC - Interact was started in year 2014 in cooperation with the two companies “Intel Mobile Communications Austria GmbH.” and “Lantiq A GmbH.” Lantiq A GmbH. and Intel Mobile Communications Austria GmbH were merged in November 2015 to “Intel Austria GmbH”. Therefore the two project partners of Interact are now the “Connected Home Division” and ”Communication & Devices Division” of Intel Cooperation, both located in Villach. The close cooperation of Interact with an important international company enables leading edge research in Austria, based on the economically and socially relevant topic of mobile communication.

A new Austrian research center for Microelectronics “Silicon Austria Labs - SAL” has been announced and is now in the start-up phase. One research focus of SAL will be related to RF circuits and systems. Therefore the JRC - Interact research topics perfectly fits to the SAL targets. A future cooperation with SAL as a continuation of the Interact research activities after completion is a clear target.

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